10 GHz Quadrature-Phase Voltage Controlled Oscillator and Prescaler

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Abstract

In this paper, a 10 GHz quadrature phase LC-VCO with a novel ring-array based injection-locked prescaler are presented. Fabricated in a 0.18 μm digital CMOS process, output frequency of VCO ranges from 10.03-9.35 GHz, and the prescaler performs divide-by 8 operation with locking range of 1 GHz. The measured phase noise from a 9.395 GHz carrier is –120 dBc/Hz at 5 MHz offset. Operating under a single 1.8 V supply, the VCO and prescaler respectively consume 21.6 mW and 12.6 mW only. Chip size are 1682.8 μm x 647.8μm.

1. Introduction

PLL-based signal generators are widely utilized as clocking sources in wireless and serial link transceivers. With the growing demands in broad-band data access to internet, carrier frequency for wireless local area network (WLAN) has been pushed beyond 5 GHz [1], while the clock multiplying units (CMU) in fiber transmitter are required to operate beyond 10 GHz [2]. In a PLL, VCO and prescaler, which operate at the highest frequency, in general dissipate the major power. Also, they are the key components that limit the achievable frequency range of PLLs. In this context, to explore circuit techniques for high frequency VCO and prescaler while maintaining low power dissipation motivates the research of this work.

In VCO design, phase noise performance, frequency tuning range and power consumption are major considerations. LC type oscillators are superior candidates to achieve low noise for the inherent bandpass filtering of LC resonator can suppress side-band noise. Conventionally, VCO’s output frequency is varied by tuning on-chip varactor diodes. However, for multi-GHz applications, varactor diodes should exhibit low parasitic capacitance and wide tuning range to cope with process variations. However, wide-tuning range is difficult to achieve under low supply voltage. In this paper, a varactorless LC-VCO with switched-tuning technique is adopted [3][4]. This VCO manifests wide tuning range to cope with process variations, while maintaining low phase noise performance. In addition, it inherent provides quadrature output phases, which are important features for phase adjustments and synchronization in transceivers.

High speed CMOS frequency dividers can be categorized into two folds; one is static divider [5], and the other is injection-locked frequency divider (ILFD) [6]-[8]. Static dividers are capable of operating at extremely wide bandwidth. However, its power consumption increases drastically along with the increments of operating frequency. On the contrary, ILFDs are capable of very high frequency operation while dissipating relatively low power, but their locking range is narrow. Since most wireless and high speed serial link-transceivers are narrow band, injection-locked dividers are viable solutions for low power and high frequency applications.

In this paper, we propose a novel ring-array based ILFD for modulo 8 operation. By means of the ring array structure, multi-phase outputs can be derived from the injection locked oscillator without sacrificing its oscillation frequency. Thus high-speed operation as well as wide locking range can be achieved with divide ratio up to 8.

2 Varactorless Quadrature Phase Oscillator

![Figure 1. Quadrature phase oscillator architecture](image_url)

Fig 1 shows the VCO architecture. The quadrature phase VCO comprises two mutually-coupled fixed frequency LC-oscillators [4]. Frequency tuning is achieved by varying the coupling coefficient (β) between two oscillators. Different from the prior art in [4], oscillation frequency is adjusted along with loop gain compensation (α). This mechanism ensures that current...
injected into LC tank remains constant regardless of frequency tuning. Thus AM-to-PM phase noise conversion can be suppressed.

Assume the two fixed frequency oscillators are identical and frequency synchronized in the stable state, X and Y are the output phasors for oscillator 1 and 2, H(jω) is the loop gain, we have
\[
(αX - βY)H(jω) = X \quad (1)
\]
\[
(αY + βX)H(jω) = Y \quad (2)
\]
It can be shown that
\[
X = ± j Y \quad (3)
\]
Therefore, quadrature outputs can be derived from X and Y. The oscillation frequency can be derived by substituting X = ± j Y into equation (1) or (2), we have
\[
(α ± j β)H(jω) = 1 \quad (4)
\]
Equation (4) governs the frequency transfer characteristic of the quadrature phase VCO. As OSC’s close loop phase response is varied by adjusting α/β, VCO’s output frequency can be changed accordingly.

The detailed circuit schematic of the VCO is shown in figure 2, which consists of two identical oscillators OSC1 (M1, M2, M9, L1, L2) and OSC2 (M5, M6, M12, L3, L4). These two oscillators are mutually coupled by two differential amplifiers (M3, M4, M10) and (M7, M8, M11). OSC’s loop gain is compensated by adjusting gate biased of M9 and M12 (α), and the coupling coefficient (β) is determined by the current source M10 and M11. In addition, 4 MOSFET capacitors Cb1- Cb4 are employed for switched-band coarse tuning.

The control signal Vfc is fully differential and derived from a tuning circuit as shown in figure 3. The tuning circuit degenerates VCO conversion gain for low noise performance. On the other hand, by means of the constant current biased scheme, α and β are reciprocal to maintain constant output power of VCO.

In order to avoid loss of coupling at the extreme case of frequency tuning, an extra current source Iα1 - Iα4 are added in parallel to current source M9-M12. Thus, quadrature output phases can be maintained at any output frequency.

3. Generic Modulo-N Injection Locked Divider

In [6], we presented a generic ring-oscillator based injection locked frequency divider, which can achieve high frequency operation with a dedicated divide ratio. And most important of all, locking range of the proposed ILFD can be drastically improved compared to the prior art in [7] by increasing its injection efficiency.

Figure 4 shows the generic ILFD architecture for modulo-N operation. The ILFD consists of n delay stages, and the incident signal is injected to all the delay cells. When the loop is in locked, two criteria are met simultaneously. One is that the input node of injector (Vx) should be synchronized with the incident signal VRF (@ωi). The other is the Barkhausen criterion for the oscillation to sustain. Assume
\[
Vj = A \sin [ωo t + (2πj / n)] \quad (j=1,2..n)
\]
It has been proven in [6] that the lowest operating frequency that can be sustained at Vx is N-th order harmonic of Vj, and all the other low-order harmonic tones are suppressed. It turns out that an N-stage ring-oscillator based ILFD, which has N output phases, is feasible for an modulo-N operation. And the achievable locking frequency would be N times higher than the free-running frequency of ring oscillator, provided the incident signal is effectively injected. Therefore, by means of
increasing the number of N in a ring-type ILFD, it stands to reason that the locking frequency as well as divide ratio can be increased accordingly. Based on this logic, ring-array-based ILFD is proposed. The ILFD’s phase number is increased by phase interpolation without seriously degrading its free running frequency. Thus both input frequency and divide ratio can be increased simultaneously.

4. Ring-Array Based Modulo-8 ILFD

The architecture of a modulo-8 ILFD is as shown in figure 5, which consists of two mutually coupled ring oscillators. Divider input signal (RF) is injected into the 4 delay cells to modulate ILFD’s oscillation frequency. Let the oscillation frequency of ILFD be \( \omega_o \). When the loop is locked, 8 evenly distributed output phases can be derived from the ring array. Similar to a single ring ILFD, the input node of ILFD is synchronized to \( \omega_{RF} \), while other harmonics of \( \omega_o \) will be suppressed. Therefore, under steady state, \( \omega_o = \omega_{RF} / 8 \).

5. Experimental results

The experimental prototype of the quadrature phase VCO along with modulo-8 ILFD have been fabricated in a 0.18 \( \mu \)m digital CMOS process. For ease of measurement, a divide-by 64 ripple counter is cascaded at the output of the ILFD prescaler. The bare die is mounted on a FR-4 PC board without packaging for test.

Figure 7 shows the measured phase noise performance from a 9.395 GHz carrier. The phase noise is –120 dBC/Hz at 5 MHz offset, and is about –106 dBC/Hz at 1 MHz offset.
Frequency tuning characteristics of the proposed VCO are summarized in figure 9. By means of switched-band tuning, VCO’s output frequency ranges from 10.03 GHz to 9.35 GHz. Each sub-band has 150 MHz overlap to cope with process and temperature variations. The effective conversion gain is about 233 MHz/V.

When the VCO is free running at 9.984GHz, the measured divider’s output is shown in figure 10. The prescaler along with ripple counter performs divide-by-512 operation, and the divider output corresponds to a 19.5 MHz clock waveform. The prescaler achieves about 1GHz locking range.

Figure 11 shows the chip micrograph. VCO and prescaler respectively occupy a chip area of 650.2 μm x 423.2 μm and 216.8 μm x 423.2 μm. Two symmetrical inductors are employed in the VCO core. And the inter stage buffer between VCO and ILFD also utilizes inductive loads to enhance its voltage swing and switching speed. Operating under a single 1.8 V supply, the VCO drains 12 mA, and prescaler dissipates 7 mA only.

6 Conclusion

In this paper, a 10 GHz varactorless quadrature phase VCO and a modulo-8 prescaler are proposed. By means of gain compensation and switched-tuning technique, the proposed VCO manifest improved phase noise and wide tuning range compared to the prior art [4].

Moreover, a ring-array based ILFD is proposed. This novel architecture achieves both high frequency operation and high divide ratio simultaneously, while consuming less power compared to static dividers.

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7. References

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