ESD Protection Design of Low-Voltage-Triggered p-n-p Devices and Their Failure Modes in Mixed-Voltage I/O Interfaces With Signal Levels Higher Than VDD and Lower Than VSS

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Abstract—Electrostatic discharge (ESD) protection design for mixed-voltage I/O interfaces with the low-voltage-triggered p-n-p (LVTp-n-p) device in CMOS technology is proposed. The LVTp-n-p, by inserting N+ or P+ diffusion across the junction between N-well and P-substrate of the p-n-p device, is designed to protect the mixed-voltage I/O interfaces for signals with voltage levels higher than VDD (over-VDD) and lower than VSS (under-VSS). The LVTp-n-p devices with different structures have been investigated and compared in CMOS processes. The experimental results in a 0.35-µm CMOS process have proven that the ESD level of the proposed LVTp-n-p is higher than that of the traditional p-n-p device. Furthermore, layout on LVTp-n-p device for ESD protection in mixed-voltage I/O interfaces is also optimized in this work. The experimental results verified in both 0.35- and 0.25-µm CMOS processes have proven that the ESD levels of the LVTp-n-p drawn in the multifinger layout style are higher than that drawn in the single-finger layout style. Moreover, one of the LVTp-n-p devices drawn with the multifinger layout style has been used to successfully protect the input stage of an asymmetric digital subscriber line (ADSL) IC in a 0.25-µm salicided CMOS process.

Index Terms—Electrostatic discharge (ESD), human body mode (HBM), low-voltage-triggered p-n-p (LVTp-n-p), optical-beam-induced resistance change (OBIRICH), photon emission microscope (EMMI).

I. INTRODUCTION

To improve circuit operating speed and performance, device dimensions of MOSFET had been shrunk in advanced CMOS technology. In order to follow the constant-field scaling requirement and to reduce power consumption, the power-supply voltages in CMOS ICs have been also scaled downwards. So, a complex microelectronics system often meets the interfaces of semiconductor chips or subsystems with different internal power-supply voltages. With the different power-supply voltages in an electronic system, the I/O interface circuit and electrostatic discharge (ESD) protection circuit must be designed to avoid electrical overstress across the gate oxide [1], to avoid hot-carrier degradation [2] on the output devices, and to prevent undesirable leakage current paths between the chips [3], [4].

One of the mixed-voltage circuit applications, such as the interface in asymmetric digital subscriber line (ADSL), which has input signals with voltage levels higher than VDD and lower than VSS, is shown in Fig. 1. The traditional on-chip ESD protection circuits are not suitable for such mixed-voltage interfaces. The ESD diode $D_p$ ($D_n$) will be forward biased when the input-signal levels are higher than VDD (lower than VSS). This ESD protection circuit will cause current leakage between the chips of the mixed-voltage I/O interface. Moreover, traditional on-chip ESD protection with NMOS/PMOS will also cause the same leakage issue and suffer the gate-oxide reliability issue when the over-VDD or under-VSS external signals reach the input pad. To meet such mixed-voltage I/O interface, the SCR device with floating P-well structure in an N-substrate CMOS process had been used as on-chip ESD protection device [5]. However, the SCR device with a floating-well structure is very sensitive to latchup [6], [7]. The mixed-voltage I/O interfaces in the system applications often have serious overshooting or undershooting signal transition, which could trigger on the SCR device in the ESD protection circuit of the I/O pad to induce latchup troubles to the chip [5].

In this work, a new ESD protection design with the low-voltage-triggered p-n-p (LVTp-n-p) device has been developed.
in Fig. (b)–(f) are proposed and investigated in this work to find the optimized design for ESD protection [8].

With the same device dimension of 30 \( \mu \text{m} \times 30 \mu \text{m} \) (the 110 width is defined as 30 \( \mu \text{m} \)) for all devices, the corresponding 111 TLP-measured I–V curves among those devices under PS-mode 112 and NS-mode stress conditions are shown in Fig. (a) and (b), 113 respectively. The secondary breakdown currents (It2) among 114 these devices are somewhat different, which could be caused by 115 the different current distribution along the devices of different 116 structures during ESD stress. Basically, the device with the 117 more effective device width will present a higher ESD robust- 118 ness. To further improve ESD level of such LVTp-n-p devices, 119 the layout to increase effective device width will be studied and 120 optimized in the next section.

B. Layout Parameters of LVTp-n-p Devices on Human Body Mode (HBM) ESD Levels

Under the 0.35-\( \mu \text{m} \) CMOS process without any extra mask 124 layer, the ESD levels among the proposed LVTp-n-p devices 125 with different layout parameters are compared in Fig. (a)–(g). 126

The layout parameters include the width or spacing, \( L_X, L_C, X, Y, S, L_1, \text{and } L_2 \), which have been indicated in Fig. (a)–(f). 128 For the gated LVTp-n-p device, the \( L_1 \) and \( L_2 \) are changed 129 simultaneously in the layout.

In Fig. (a) and (b), as the width of the LVTp-n-p devices is 131 increasing, the HBM ESD levels are improved under both 132 positive-to-VSS and negative-to-VSS ESD-stress conditions. 133 This confirms that when the area of effective ESD current flow 134 from emitter to collector is increased, the heat will be dissipated 135 through the larger region. Therefore, the device can sustain a 136 higher ESD level.

In Fig. (c), as the spacing \( X \) of the type LVTp-n-p or 137 the spacing \( Y \) of the type LVTp-n-p is increasing, the HBM 139 ESD level is improved under the positive-to-VSS ESD-stress 140 condition. Here, the LVTp-n-p devices, with the increase of 141 \( X \) or \( Y \), will have a wider field oxide region in the device 142 structures, but the N+ or P+ diffusion across the N-well/143 P-substrate junction is kept, to have the same diffusion layout 144 spacing of 1.2 \( \mu \text{m} \). The TLP-measured I–V curves of the type 145 LVTp-n-p with different \( X \) spacings and the type LVTp-n-p 146 with different \( Y \) spacings are shown in Fig. (a) and (b), 147 respectively. As these spacings increase, the clamped voltage 148 across the devices will be increased due to the increased turn-149 on resistances. The voltage drop across the base–collector 150 (B–C) junction will increase to cause the emitter–base (E–B) 151 potential barrier to be lowered. The lowering potential barrier 152 at the E–B junction produces a large increase in current with 153 a very small increase in B–C voltage. This effect is the so- 154 called punchthrough breakdown phenomenon [13], which will 155 occur before the avalanche breakdown. In Fig. (d), as the 156 spacing \( S \) of the LVTp-n-p is increasing, the HBM ESD level is 157 improved under the negative-to-VSS ESD-stress condition. 158 This ESD-stress condition, however, the parameter \( S \) plays the 159 same role as parameters \( X \) and \( Y \) in the positive-to-VSS ESD- 160 stress condition. Because these spacings increase, the voltage 161 drop across the base–Emitter (B–E) junction will increase to 162 cause the collector–Base (C–B) potential barrier to be lowered.

### A. Device Structures and TLP-Measured I–V Characteristics

The cross-sectional view of the traditional p-n-p device in an 101 N-well/P-substrate CMOS process is shown in Fig. (a), where 102 the N-well is floating in this structure to avoid the leakage 103 path from the pad to grounded P-substrate. The P+ diffusion 104 (emitter) in the floating N-well is connected to the I/O pad for 105 ESD protection. By inserting N+ or P+ diffusion across the 106 junction between the N-well and P-substrate of the traditional 107 p-n-p device, five new different structures of LVTp-n-p devices

Fig. 2. New proposed ESD protection design with LVTp-n-p device for the mixed-voltage I/O interface with input voltage levels higher than VDD and lower than VSS. 69 to protect the I/O interfaces with input voltage levels higher 70 than VDD or lower than VSS [8]. Comparing to the traditional 72 LVTp-n-p with a low breakdown voltage, by avalanche break- 73 down across the P+/N-well or N+/P-subjunctions, provides an 74 effective discharging path to protect the mixed-voltage I/O 75 interfaces against ESD stresses. Under normal circuit oper- 76 ation conditions, the LVTp-n-p device is kept off without 77 causing current leakage between the chips. Furthermore, lay- 78 out optimization on the LVTp-n-p device to increase its ESD 79 robustness per silicon area has been also studied [9]. The 80 multifinger layout style is used to improve ESD robustness 81 of the LVTp-n-p device. Moreover, the input stage of ADSL 82 protected by the LVTp-n-p device has been practically imple- 83 mented in a 0.25-\( \mu \text{m} \) salicided CMOS process to achieve a 84 better ESD robustness.
Therefore, the lowering potential barrier at the C–B junction produces a large increase in current, but with a very small increase in B–E voltage. From such results, these spacings in LVTp-n-p devices can be further optimized in layout to improve ESD robustness for applications in such mixed-voltage I/O interfaces.

In Fig. 5(e), as the \( L_E \) of the LVTp-n-p devices is increasing, the HBM ESD level is improved under the negative-to-VSS ESD-stress condition. Because the heat will be located around the B–E junction, as the emitter junction area is increased, the heat will be dissipated through the larger region. However, under the positive-to-VSS ESD-stress condition, this parameter has no influence on the ESD level, because the heat will be located around the B–C junction with the same area in the test chips.

The parameter \( L_C \) of the LVTp-n-p devices almost has no influences on the HBM ESD level. Under both positive-to-VSS and negative-to-VSS ESD-stress conditions, the heat will be located around B–C and B–E junctions, respectively. However, the heat will not be located around the P+ diffusion in the P-substrate.

In Fig. 5(f), as \( L_1 \) of the gated1 LVTp-n-p (\( L_1 \) and \( L_2 \) of the gated2 LVTp-n-p) is increasing, the ESD level is improved under the positive-to-VSS ESD-stress condition. In Fig. 5(g), as \( L_1 \) and \( L_2 \) of the gated2 LVTp-n-p is increasing, the ESD level is improved under the negative-to-VSS ESD-stress condition. However, in such ESD-stress mode, \( L_1 \) has no influence to the ESD level of both gated1 LVTp-n-p and gated2 LVTp-n-p. Such layout parameters \( L_1 \) (\( L_2 \)) in the gated LVTp-n-p play the same role as that of the parameters \( X(S) \) in the type1 LVTp-n-p, as well as the parameters \( Y(S) \) in the type2 LVTp-n-p. By correctly adjusting the layout parameters, the desired ESD level of the mixed-voltage I/O interface can be achieved by the proposed LVTp-n-p devices with the optimized layout parameters.

C. Multifinger Layout Style for LVTp-n-p to Improve ESD Robustness

The ESD robustness of the LVTp-n-p device with the single-finger layout style, which is shown in Fig. 7(a), and its cross-sectional view shown in Fig. 7(b), cannot meet the ESD specification of 2-kV HBM ESD level in a limited silicon area. Therefore, based on the dependence of ESD levels on the layout parameters (including the width, \( L_E \), \( L_C \), \( X \), \( Y \), \( S \)) of LVTp-n-p devices, the ESD level mainly depends on the effective device width from its emitter to its collector in both PS- and NS-mode ESD stresses. On the other hand, \( L_E \) affects only the NS-mode ESD level and \( L_C \) does not affect the ESD level. However, comparing the PS- and NS-mode ESD levels,
The LVTp-n-p devices drawn with the single-finger layout style and the new proposed multifinger layout style have been fabricated in both 0.35-\(\mu\)m polycided and 0.25-\(\mu\)m salicided CMOS processes without any extra additional mask layer. Under the positive-to-VSS ESD-stress condition, the HBM ESD levels of the LVTp-n-p devices with the single-finger and multifinger layout styles are compared in Table I. In almost the same layout area, the LVTp-n-p devices with the multifinger layout style have much higher ESD robustness than those with the single-finger layout style in both 0.35-\(\mu\)m polycided and 0.25-\(\mu\)m salicided CMOS processes. Specifically, the type3 LVTp-n-p with multifinger layout has 247 the highest ESD robustness, which can sustain an HBM ESD stress of 3.3 kV in the 0.35-\(\mu\)m polycided CMOS process and 249 3.8 kV in the 0.25-\(\mu\)m salicided CMOS process. Furthermore, 250 within unit layout area, the ESD robustness of type3 LVTp-n-p 251 is increased from 0.59 to 2.69 V/\(\mu\)m\(^2\) in the 0.35-\(\mu\)m polycided 252 CMOS process and from 1.71 to 3.10 V/\(\mu\)m\(^2\) in the salicided 253 0.25-\(\mu\)m CMOS process. With suitable selection on the 254 LVTp-n-p devices and layout style, the overall ESD robustness 255 of the mixed-voltage I/O interfaces can be designed to meet 256 the ESD specification of 2-kV HBM ESD level within 257 a smaller silicon area. Specifically, the LVTp-n-p in the type3 258 device structure with multifinger layout style has excellent 259 ESD performance.

Because the doping concentration in the 0.25-\(\mu\)m salicided 261 CMOS process is higher than that in the 0.35-\(\mu\)m polycided 262 CMOS process, the junctions have slightly lower breakdown 263 voltages in the 0.25-\(\mu\)m CMOS process than that in the 0.35-\(\mu\)m 264 CMOS process. With the single-finger layout style, HBM ESD 265 levels of the LVTp-n-p devices in the 0.25-\(\mu\)m CMOS process 266 are higher than those of the LVTp-n-p devices in the 0.35-\(\mu\)m 267 CMOS process under both positive-to-VSS and negative-to-VSS 268 ESD-stress conditions. Moreover, HBM ESD levels of the 269 LVTp-n-p devices in the 0.25-\(\mu\)m CMOS process are higher 270 than those of the LVTp-n-p devices in the 0.35-\(\mu\)m CMOS 271 process under negative-to-VSS ESD-stress condition, when 272 they are drawn with the multifinger layout style. However, 273 HBM ESD levels of the LVTp-n-p devices in the 0.25-\(\mu\)m salicided 274 CMOS process are lower than those of the LVTp-n-p devices 275 in the 0.35-\(\mu\)m polycided CMOS process under 276 positive-to-VSS ESD-stress condition for the multifinger lay- 277 out style. The silicided diffusion in the 0.25-\(\mu\)m salicided 278 CMOS process causes degradation on ESD robustness of the 279 LVTp-n-p device drawn in multifinger layout style [14]. Under 280 ESD-stress condition, the silicide diffusion on the device will 281 cause the current to be crowded on the surface of the device 282 and the heat will be located in the local area. To further increase 283 the ESD level of the LVTp-n-p device in the 0.25-\(\mu\)m salicided 284 CMOS process, the optional silicided-blocking mask layer can 285 be used to block the silicide formation around the perimeter of 286 the emitter region of the LVTp-n-p device.

Moreover, the TLP-measured I–V curves of LVTp-n-p devices 288 with the single-finger layout style and the multifinger layout 289 style in the 0.25-\(\mu\)m salicided CMOS process under 290 PS-mode and NS-mode stress conditions are compared in Fig. 9(a) and (b), respectively. Due to the increase of total 292 effective device width and the decrease of the length from 293

![TLP-measured I–V curves among traditional p-n-p and different LVTp-n-p devices under (a) the positive-to-VSS (PS-mode), and (b) the negative-to-VSS (NS-mode) stress conditions.](image-url)
Fig. 5. (a) ESD level versus device width under the positive-to-VSS ESD-stress condition. (b) ESD level versus device width under the negative-to-VSS ESD-stress condition. (c) ESD level versus the spacing $X$ of the type1 LVTp-n-p or the spacing $Y$ of the type2 LVTp-n-p under the positive-to-VSS ESD-stress condition. (d) ESD level versus the spacing $S$ under the negative-to-VSS ESD-stress condition, respectively. (e) ESD level versus device $L_E$ under the negative-to-VSS ESD-stress condition. (f) ESD level versus $L_1$ or $L_2$ of the gated1 LVTp-n-p and the gated2 LVTp-n-p under the positive-to-VSS ESD-stress condition. (g) ESD level versus $L_1$ or $L_2$ of the gated1 LVTp-n-p and the gated2 LVTp-n-p under the negative-to-VSS ESD-stress condition.

its emitter to its collector, the LVTp-n-p devices with the multifinger layout style have lower turn-on resistances than those with the single-finger layout style in the same layout area. Hence, the $I_{t2}$ of LVTp-n-p devices with the multifinger layout style is higher than those with the single-finger layout style. For the single-finger layout style, however, because the turn-
Fig. 6. TLP-measured $I-V$ curves of (a) the type1 LVTp-n-p with different $X$ spacings, and (b) the type2 LVTp-n-p with different $Y$ spacings, under the positive-to-VSS stress condition.

Fig. 7. (a) Single-finger layout style of the LVTp-n-p, and (b) cross-sectional view along the line AA’ in the single-finger layout of LVTp-n-p.

Fig. 8. (a) Multifinger layout style of the LVTp-n-p, and (b) cross-sectional view along the line BB’ in the multifinger layout of LVTp-n-p.
### TABLE I
HBM ESD Levels of the LVTp-n-p Devices with Different Layout Styles under Positive-to-VSS ESD-Stress Condition

<table>
<thead>
<tr>
<th>Device Layout Style</th>
<th>Type1 Single Finger Layout</th>
<th>Type2 Single Finger Layout</th>
<th>Type3 Single Finger Layout</th>
<th>Type1 Multi-Finger Layout</th>
<th>Type2 Multi-Finger Layout</th>
<th>Type3 Multi-Finger Layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layout Area (µm×µm)</td>
<td>36×32</td>
<td>36×32</td>
<td>36×32</td>
<td>33.6×36.5</td>
<td>33.6×36.5</td>
<td>33.6×36.5</td>
</tr>
<tr>
<td>HBM ESD Level (V) in a 0.35-µm CMOS Process</td>
<td>250</td>
<td>350</td>
<td>550</td>
<td>950</td>
<td>1050</td>
<td>3.6k</td>
</tr>
<tr>
<td>HBM ESD Level (V) in a 0.25-µm CMOS Process</td>
<td>350</td>
<td>350</td>
<td>750</td>
<td>850</td>
<td>900</td>
<td>1.4k</td>
</tr>
<tr>
<td>$V_{ESD/area}$ (V/µm²) in a 0.35-µm CMOS Process</td>
<td>0.22</td>
<td>0.3</td>
<td>0.5</td>
<td>0.77</td>
<td>0.86</td>
<td>2.94</td>
</tr>
<tr>
<td>$V_{ESD/area}$ (V/µm²) in a 0.25-µm CMOS Process</td>
<td>0.3</td>
<td>0.3</td>
<td>0.68</td>
<td>0.69</td>
<td>0.73</td>
<td>1.14</td>
</tr>
</tbody>
</table>

### TABLE II
HBM ESD Levels of the LVTp-n-p Devices with Different Layout Styles under Negative-to-VSS ESD-Stress Condition

<table>
<thead>
<tr>
<th>Device Layout Style</th>
<th>Type1 Single Finger Layout</th>
<th>Type2 Single Finger Layout</th>
<th>Type3 Single Finger Layout</th>
<th>Type1 Multi-Finger Layout</th>
<th>Type2 Multi-Finger Layout</th>
<th>Type3 Multi-Finger Layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layout Area (µm×µm)</td>
<td>36×32</td>
<td>36×32</td>
<td>36×32</td>
<td>33.6×36.5</td>
<td>33.6×36.5</td>
<td>33.6×36.5</td>
</tr>
<tr>
<td>HBM ESD Level (V) in a 0.35-µm CMOS Process</td>
<td>1.2k</td>
<td>700</td>
<td>650</td>
<td>2.6k</td>
<td>2.4k</td>
<td>3.3k</td>
</tr>
<tr>
<td>HBM ESD Level (V) in a 0.25-µm CMOS Process</td>
<td>2.4k</td>
<td>2.2k</td>
<td>1.9k</td>
<td>2.7k</td>
<td>2.8k</td>
<td>3.8k</td>
</tr>
<tr>
<td>$V_{ESD/area}$ (V/µm²) in a 0.35-µm CMOS Process</td>
<td>1.04</td>
<td>0.61</td>
<td>0.59</td>
<td>2.12</td>
<td>1.96</td>
<td>2.69</td>
</tr>
<tr>
<td>$V_{ESD/area}$ (V/µm²) in a 0.25-µm CMOS Process</td>
<td>2.08</td>
<td>1.91</td>
<td>1.71</td>
<td>2.20</td>
<td>2.28</td>
<td>3.10</td>
</tr>
</tbody>
</table>
flow from \( R \) and \( R_1 \) to \( V_c \), the voltage level at the differential input will be divided by \( R \) and \( R_1 \). During ESD stress, if the divided voltage level on the differential input is larger than the gate-oxide breakdown voltage of the input NMOS, the ESD stress will damage the gate oxide of the input NMOS. By using the proposed ESD protection design with LVTp-n-p, the ESD current will discharge through the LVTp-n-p to VSS. Because the \( V_t2 \) of the LVTp-n-p is lower than the voltage drop on \( R \) pulsing the gate-oxide breakdown voltage of NMOS, the ESD gate oxide of the input NMOS can be successfully protected in this ADSL interface. By the way, the input node \((V_{i1})\) of the opamp in Fig. 10(a) is also connected to its output \((V_o)\) through the feedback resistor \( R_f \), which will also help to clamp the overshooting voltage on the gate oxide of the input stage. To reduce the \( V_t2 \) at a given current level, the device width should be further increased to have a lower turn-on resistance. Among the LVTp-n-p devices, the type3 LVTp-n-p is selected for input ESD protection design in ADSL interface due to its highest HBM ESD level. In Fig. 10, the type3 LVTp-n-p device 353 is connected between the input pad and VSS power line, and the power-rail ESD clamp circuit is realized by the \( RC \)-inverter- NMOS circuit [10]. The layout views of the ADSL input stage without and with ESD protection circuit are shown in Fig. 11(a) and (b), respectively. When ESD stress occurs at the input pin, the type3 LVTp-n-p will break down with a lower trigger voltage to discharge ESD current. With the power-rail ESD 360 clamp circuit, the PS, NS, PD, and ND ESD stresses can be 361 discharged through the type3 LVTp-n-p to VSS or VDD. Under 362 PS-mode ESD-stress condition, the ESD current will flow from 363 the input pad through LVTp-n-p to VSS. Under NS-mode ESD- 364 stress condition, the ESD current will flow from VDD through 365 LVTp-n-p to the input pad. Under PD-mode ESD-stress condition, the ESD current will flow from the input pad through 367 LVTp-n-p to VSS, and then through the power-rail ESD clamp 368 circuit to VDD. Under ND-mode ESD-stress condition, the 369 ESD current will flow from VDD through the power-rail ESD 370 clamp circuit to VSS or VDD, and finally from \( V_o \) through the parasitic 380 diode (drain–N-well p-n junction) of \( M_6 \) in the single-ended 381 opamp to VDD, and finally from VDD through the path 382 of \( M_2-M_1-M_3 \) to VSS or through the bias circuit to VSS. Due to the turn-on bias circuit, \( M_7 \) will turn on. Therefore, before ESD stress, there is current flow from input through the internal circuits to VSS when applying a signal to the input pad. Due to the reason of initial current, to compare the ESD protection ability, the input stage of ADSL without and with the ESD protection circuit has been tested in HBM ESD stress with the failure criterion of 30% shifting on the voltage at 1-\( \mu \)A.

**B. HBM ESD Levels of ADSL With the Type3 LVTp-n-p**

When applying a positive bias (with VSS grounded and VDD floating) to the input pad of ADSL, the current will flow 379 from \( R \) and \( R_1 \) to \( V_c \), and then from \( V_c \) through the parasitic 380 diode (drain–N-well p-n junction) of \( M_6 \) in the single-ended 381 opamp to VDD, and finally from VDD through the path 382 of \( M_2-M_1-M_3 \) to VSS or through the bias circuit to VSS. Due to the turn-on bias circuit, \( M_7 \) will turn on. Therefore, before ESD stress, there is current flow from input through the internal circuits to VSS when applying a signal to the input pad. Due to the reason of initial current, to compare the ESD protection ability, the input stage of ADSL without and with the ESD protection circuit has been tested in HBM ESD stress with the failure criterion of 30% shifting on the voltage at 1-\( \mu \)A.
Fig. 10. (a) ESD protection design for the ADSL input stage with single-ended opamp and voltage divider in a 0.25-μm salicided CMOS process. (b) Schematic of the two-stage opamp.

Fig. 11. Layout views of the ADSL input stage (a) without ESD protection, and (b) with ESD protection circuit.

Fig. 12. $I-V$ curves of the ADSL input stage with ESD protection circuit before and after PS-mode HBM ESD stress of 1.5 kV, which was measured by applying a swept voltage from $-1$ to $5$ V on the input pad with VSS grounded and VDD floating.

I–V curves of the input stage of ADSL with ESD protection circuit before and after the HBM PS-mode ESD stress of 1.5 kV are shown in Fig. 12, which was measured by applying a swept voltage from $-1$ to $5$ V on the input pad with VSS grounded and VDD floating. Before ESD stress, while the input pad is swept from 0 to 5 V with grounded VSS (VDD floating), the signal current bias from its original $I-V$ curve [15]–[17]. The typical $I-V$ curves of the input stage of ADSL with ESD protection circuit before and after the HBM PS-mode ESD stress of 1.5 kV are shown in Fig. 12, which was measured by applying a swept voltage from $-1$ to $5$ V on the input pad with VSS grounded and VDD floating. Before ESD stress, while the input pad is swept from 0 to 5 V with grounded VSS (VDD floating), the signal...
TABLE III
HBM ESD LEVELS OF THE ADSL INPUT STAGE WITH DIFFERENT ESD PROTECTION DESIGNS UNDER PS-, NS-, PD-, AND ND-MODE ESD-STRESS CONDITIONS

<table>
<thead>
<tr>
<th></th>
<th>PS-Mode (Positive-to-VSS)</th>
<th>NS-Mode (Negative-to-VSS)</th>
<th>PD-Mode (Positive-to-VDD)</th>
<th>ND-Mode (Negative-to-VDD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADSL Only</td>
<td>450V</td>
<td>350V</td>
<td>450V</td>
<td>400V</td>
</tr>
<tr>
<td>ADSL Including the Type3 LVTPNP with Single Finger Layout Style</td>
<td>750V</td>
<td>1.9kV</td>
<td>750V</td>
<td>1.9kV</td>
</tr>
<tr>
<td>ADSL Including the Type3 LVTPNP with Multi-Finger Layout Style</td>
<td>1.4kV</td>
<td>3.8kV</td>
<td>1.3kV</td>
<td>3.8kV</td>
</tr>
</tbody>
</table>

paths will flow into the opamp circuit. Therefore, the $I$–$V$ curve will become a straight line, with a slope equal to the reciprocal of $R + R_I$, which starts at the voltage drop of internal circuits. Moreover, before ESD stress, while the input pad is swept from $0$ to $-1$ V with grounded VSS (VDD floating), the input current will flow from VSS through the parasitic diode of $M_7$ in the single-ended opamp, and then through $R_I$ and $R$ to the input pad. Therefore, the $I$–$V$ curve will become a straight line, with a slope equal to the reciprocal of $R + R_I$, which starts at the cut-in voltage of the parasitic diode of $M_7$. However, after an HBM ESD stress of 1.5 kV, the type3 LVTp-n-p is burned out to cause a short circuit line in the $I$–$V$ curve.

The input stage of ADSL protected by the type3 LVTp-n-p devices in the single-finger layout style or the multifinger layout style and the power-rail ESD clamp circuit has been fabricated in a 0.25-$\mu$m salicided CMOS process. The HBM ESD levels of the ADSL input stage under PS-, NS-, PD-, and ND-mode ESD-stress conditions are shown in Table III. The LVTP-n-p in single-finger layout style is drawn with a device size of 36 $\mu$m x 32 $\mu$m, whereas the LVTp-n-p in the multifinger layout style is drawn with a device size of 33.6 $\mu$m x 36.5 $\mu$m. As seen in Table III, with the type3 LVTp-n-p and the power-rail ESD clamp circuit, the input stage of ADSL indeed can be protected from ESD stress. Moreover, HBM ESD levels of the input stage of ADSL protected by the LVTP-n-p in multifinger layout style are higher than those of the input stage of ADSL protected by the LVTP-n-p in single-finger layout style. To further increase ESD level, the layout of the LVTP-n-p should be improved with the multifinger layout style, or the silicide-blocking mask layer should be used to block the silicide formation around the perimeter of emitter region of the LVTP-n-p device.

C. Failure Analysis

The photon emission microscope (EMMI) picture of the ADSL input stage without ESD protection circuit after HBM PS-mode ESD stress of 500 V is shown in Fig. 13. The ESD damage, indicated by the arrow, is located on the opamp of the ADSL input stage.

In the layout of the ADSL input stage protected by the type3 LVTp-n-p, the type3 LVTp-n-p is fully covered by the metal layers on the top. The ESD damage on the device junction cannot be observed by the EMMI picture. Here, the optical beam-induced resistance change (OBIRCH) [18], [19] is used to find the ESD-damage location on the input stage of ADSL with ESD protection circuit after HBM PS-mode ESD stress. The OBIRCH picture shown in Fig. 14 indicates the ESD damage located on the type3 LVTp-n-p device after 1.5-kV HBM PS-mode ESD stress. From the failure location in Fig. 14, the type3 LVTp-n-p indeed is triggered ON to conduct ESD current to effectively protect the mixed-voltage I/O interface of the ADSL input stage.

III. Conclusion

ESD protection design for the mixed-voltage I/O interfaces with new proposed LVTP-n-p devices has been successfully verified to achieve a good ESD protection in a 0.35-$\mu$m CMOS process. The proposed LVTP-n-p devices have a higher ESD level than that of the traditional p-n-p device. Moreover, the
Fig. 14. OBIRCH picture on the ADSL input stage with ESD protection circuit after 1.5-kV HBM PS-mode ESD stress. The failure location is on the type 3 LVTp-n-p device of the ESD protection circuit.

multifinger layout style has been used to increase the effective device width among the LVTp-n-p device for improving ESD robustness in both 0.35- and 0.25-µm CMOS processes. Comparing among these LVTp-n-p devices, the type 3 LVTp-n-p in the multifinger layout style can sustain the highest ESD stress for application in the mixed-voltage I/O interfaces. ESD protection codesigned with the LVTp-n-p device and the powerrail ESD clamp circuit has been successfully implemented to protect the ADSL input stage in a 0.25-µm salicided CMOS process.

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REFERENCES


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